detecting coincidence of plurality of bits for each predetermined group of image data outputted by the data supply circuit (claim 14)."

In the Office Action, the Examiner rejects claims 1-18 under 35 U.S.C. §103(a) as being unpatentable over Shimamoto in view of Rindal [et al.] (U.S. Patent No. 5,659,339). In response to the Amendment filed on June 13, 2002, the Examiner maintains the same position, that Shimamoto fails specifically teach that the transfer of output data is performed with a time delay that lags one another. The Examiner has newly cited Rindal as allegedly teaching the time delay feature.

Shimamoto concerns conversion of serial data to parallel data to accommodate transfer of a large number of bits for high-resolution display. That is, in the Shimamoto display, signals are transferred serially at a low voltage and high speed from a display controller to a flat panel. A low voltage serial data parallel conversion circuit restores the low voltage signals, which are supplied to a flat panel driving/controlling circuit. Therefore, by reducing the signal level, display signal interface lines can be reduced as well as reducing EMI. While Shimamoto is concerned with reduction of electromagnetic wave noise, the foregoing different solution is applied to achieve it. As acknowledged by the Office Action, Shimamoto fails to disclose or suggest reducing the number of simultaneous changes of display data output signals to lower the occurrence of EMI.

Rindal discloses a method and apparatus for reducing EMI radiated by flat panel screens by periodically phase-modulating the panel clock signal into at least two phases. Conventionally, and as disclosed in the background section of Rindal, the position of data sequentially displayed on a flat panel is determined by the number of clock pulses from a reference signal, the reference signal having fast rising and falling edges much like that

of a square wave. With reference to the frequency spectral density illustrated by Fig. 2B, as the EMI reference window sweeps along the frequency axis, there will be relatively high EMI spectral energy interference. Low pass filters are used to reduce the EMI to a limited degree. Rindal discloses other methods of reducing EMI, none of which corresponds to the claimed invention.

Essentially, Rindal purports to reduce EMI by spreading-out the EMI-producing spectral energy by phase-modulating the panel clock signal. This produces a panel clock having at least two phases. As a result, adjacent spectra energy is separated by a sufficiently large frequency range, and therefore, falls outside of the EMI reference window.

Applicants have reproduced below certain features of the independent claims 1, 5, 9, and 13 of this application that are neither disclosed nor suggested by Shimamoto, Rindal, or the combination thereof.

> Claim 1 recites, *inter alia*, "points of changing said data output signals with respect to a time base are set with time delays that lag one another during one period of a reference internal clock signal, so that number of simultaneous changes of display data output signals is reduced."
>
> Claim 5 recites, *inter alia*, "points of changing said display data output signals with respect to a time base are set with time delays that lag one another during one period of a clock output signal or a reference internal clock signal having a same phase as the clock output signal, so that number of simultaneous changes of display data output signals is reduced."
>
> Claim 9 recites, *inter alia*, "red, green and blue colored display data composed of plural bits are transferred ... each transfer is performed with a time delay that lags incrementally for each bit unit formed of plural bits optionally selected from each of said display data."
>
> Claim 13 recites, *inter alia*, "a display timing control circuit for transferring red, green and blue color display data formed of plural bits to

> the TFT drive circuit...; and a delay unit provided in the displayed timing control circuit to delay the transfer timing between one bit unit and another."

EMI is typically caused by simultaneously changing each data output signal of a multi-port system, which causes a high momentary generated current. This current creates electromagnetic noise, which negatively affects other system components. By delaying data output signals from one another, as embodied by the claims, only a small current is generated by each change thereby reducing the negative effects of EMI on other system components.

The time delay feature common to independent claims 1, 4, 9, and 13, is not disclosed or suggested by the Shimamoto reference, which is acknowledged by the Examiner. The Examiner, however, references col. 6, lines 54-55, of Rindal, which states that "[t]he data may be delayed almost arbitrarily providing the panel clock signal is identically delayed." The Examiner opines that "even though, it is not stated that the data signals are delayed in a manner in which one specifically are time delayed to lag one another, it is stated that it may be delayed almost arbitrarily as long as the panel clock signal is also delayed and does not reduce the display performance." The Examiner opines further that it would have been obvious to reduce EMI by delaying the rate of data signal, whether it is a time delayed to lag one another or delayed spontaneously, as taught by Rindal, in an apparatus similar to which is taught by Shimamoto to thereby reduce EMI without significantly impacting on display performance. We disagree.

The Examiner's position is not supported by the Shimamoto or Rindal disclosure. The statement that a data clock signal may be delayed arbitrarily in accordance with a panel clock signal does not teach delaying output signals with respect to a time base with

time delays that lag one another, as the claims recite. For instance, figures 5A-4 and 5A-5 illustrate a data signal clocked in accordance with the panel clock signal. In most, and if not all, systems that output data, a data signal is outputted in accordance with a clock signal. It follows that if a panel clock signal is delayed, so should the data signal. Rindal describes this common operation, but fails to disclose or suggest the instance where more than one data signals are outputted so as to lag one another, as the claims recite.

Moreover, even if Shimamoto were altered with the teachings with Rindal, the output signals of red, green and blue would be delayed the same in accordance with a delayed panel clock signal. There is no disclosure or suggestion in Shimamoto or Rindal or from the combination thereof, that the output signals would be delayed as to lag one another, as the claims recite.

Further, the Examiner has failed to provide sufficient motivation to combine the teachings of the references. Case law precedent makes it explicitly clear that conclusionary statements made to support an obviousness rejection are improper and lack any legal basis. Contrary to precedent, the Examiner makes a conclusionary statement that the delay of a data signal in Rindal would somehow accomplish the novel feature of a time delay to lag one another for a multi-port system. Hence, the obviousness rejection is improper.

For the reasons above, independent claims 1, 5, 9, and 13 and claims dependent therefrom are patentable as Shimamoto in view of Rindal fail to disclose or suggest that points of changing data output signals with respect to a time base are set with time delays that lag one another. Further, this feature is not taught in the combinations elements that

are claimed in claims 1, 5, 9 and 13. The Examiner has acknowledged these deficiencies of the references in the Interview Summary for the interview of November 13, 2002.

Considering claim 14, there are significant features of that independent claim which are neither disclosed nor suggested by Shimamoto, Rindal, or namely among other things "a detector circuit for detecting a coincidence of polarity by comparing a polarity of bit for each predetermined group of image data outputted by the data display circuit; a first control circuit ...; and a second control circuit for outputting data ... when the coincidence of polarity of bit has been detected by the detector circuit."

The Examiner references columns 6-7, lines 56-26, respectively, alleging that the first and second control circuit of claim 14 are disclosed. Contrary to the Examiner's position, the cited portion of Shimamoto relates to the arrangement of the parallel/serial (P-S) converter. There is no disclosure or suggestion of operation with respect to a coincidence of polarity. In particular, there is no disclosure or suggestion of a detector circuit for detecting a coincidence of polarity by comparing a polarity of bit for each predetermined group of image data outputted by the data supply circuit, as claim 14 recites. Moreover, there is no disclosure or suggestion of a first and second control circuit for outputting data...when the coincidence of polarity of bit has been detected by the detector circuit, as claim 14 also recites.

Shimamoto and Rindal fail to disclose or suggest the aforementioned features of claim 14. The Examiner has acknowledged such deficiencies in the Interview Summary. For these reasons, the obviousness rejection of claim 14 and respective dependent claims is improper. Withdraw of the rejection is respectfully solicited.

As Shimamoto and Rindal, alone or in combination, fail to disclose or suggest each and every feature of claims 1, 5, 9, 13, and 14, and there is motivation is combine, the applied obviousness rejection is inappropriate. Claims dependent therefrom are patentable, at least based on their dependency and for the reasons stated above. Withdraw of the rejection is respectfully solicited. In light of the foregoing remarks, the outstanding rejection has been overcome. Applicants respectfully solicit prompt allowance of this case.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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WDC99 682456-1.050073.0019